What is claimed is:

1. A semiconductor package which has a plurality of connection terminals to be connected to a board and a plurality of test terminals on a joint surface thereof to said board,

wherein a first area where said connection terminals are arranged at predetermined pitches in a lattice and a second area where said test terminals are arranged at pitches narrower than said predetermined pitches in a lattice are placed.

2. The semiconductor package according to claim 1, wherein said connection terminals and said test terminals are formed by solder balls.

3. The semiconductor package according to claim 1, wherein said connection terminals and said test terminals are formed by lands.

4. The semiconductor package according to claim 1, wherein said second area is placed in the center of said joint surface, and said first area is placed in the periphery of said joint surface so as to surround said second area.

5. The semiconductor package according to claim 4, wherein said connection terminals and said test terminals are formed by solder balls.

6. The semiconductor package according to claim 4, wherein said

connection terminals and said test terminals are formed by lands.

7. The semiconductor package according to claim 1, wherein said second area is placed in the periphery of said joint surface, and said first area is placed so as to surround said second area.

8. The semiconductor package according to claim 7, wherein said connection terminals and said test terminals are formed by solder balls.

9. The semiconductor package according to claim 7, wherein said connection terminals and said test terminals are formed by lands.

10. The semiconductor package according to claim 7, wherein said second area is placed on layout of a high-heat-buildup circuit mounted.

11. The semiconductor package according to claim 10, wherein said connection terminals and said test terminals are formed by solder balls.

12. The semiconductor package according to claim 10, wherein said connection terminals and said test terminals are formed by lands.

13. The semiconductor package according to claim 1, wherein said first area is formed in a plurality of places, and said second area is placed so as to isolate said first areas respectively formed in said plurality of places from each other.

14. The semiconductor package according to claim 13, wherein said connection terminals and said test terminals are formed by solder balls.

15. The semiconductor package according to claim 13, wherein said connection terminals and said test terminals are formed by lands.

16. The semiconductor package according to claim 13, wherein the test terminals in said second area are mounted on ground.

17. The semiconductor package according to claim 16, wherein said connection terminals and said test terminals are formed by solder balls.

18. The semiconductor package according to claim 16, wherein said connection terminals and said test terminals are formed by lands.

19. The semiconductor package according to claim 1, wherein said second area is placed in the four corners of said joint surface, and said first area is placed in an area except for said four corners.

20. The semiconductor package according to claim 19, wherein said connection terminals and said test terminals are formed by solder balls.

21. The semiconductor package according to claim 19, wherein said

connection terminals and said test terminals are formed by lands.

22. A lead-type semiconductor package which has a plurality of connection leads to be connected to a board and a plurality of test leads,

wherein said connection leads are arranged at predetermined pitches, and said test leads are arranged at pitches narrower than said predetermined pitches.